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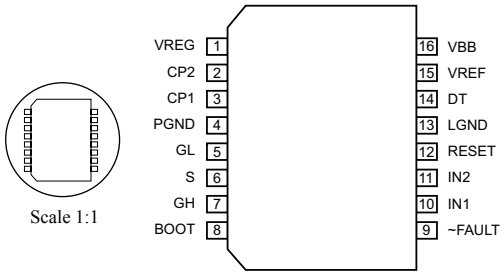
3946

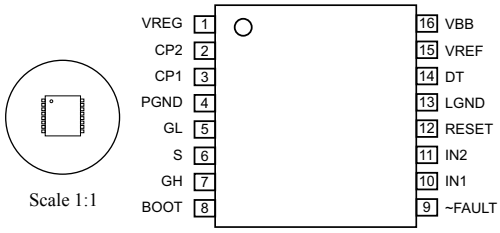
Data Sheet
29319.150

Half-Bridge Power MOSFET Controller

A3946KLB SOIC



A3946KLP TSSOP with Exposed Thermal Pad



ABSOLUTE MAXIMUM RATINGS

Load Supply Voltage, V_{BB} ..... **60 V**
Logic Inputs .....**–0.3 V to 6.5 V**
Pin S…… .....**–4 V to 60 V**
Pin GH .....**–4 V to 75 V**
Pin BOOT….. .....**–0.6 V to 75 V**
Pin DT ..... **V_{REF}**
Pin VREG .....**–0.6 V to 15 V**
Package Thermal Resistance, R_{JA}
A3946KLB..... **48°C/W**[1]
A3946KLB..... **38°C/W**[2]
A3946KLP ..... **44°C/W**[1]
A3946KLP ..... **34°C/W**[2]
Operating Temperature Range, T_A .. **–40°C to +135°C**
Junction Temperature, T_J.....**+150°C**
Storage Temperature Range, T_S....**-55°C to +150°C**

Notes:
1. Measured on a two-sided PCB with 3 in.² of 2 oz. copper.
2. Measured on JEDEC standard High-K board.

The A3946 is designed specifically for applications that require high power unidirectional dc motors, three-phase brushless dc motors, or other inductive loads. The A3946 provides two high-current gate drive outputs that are capable of driving a wide range of power N-channel MOSFETs. The high-side gate driver switches an N-channel MOSFET that controls current to the load, while the low-side gate driver switches an N-channel MOSFET as a synchronous rectifier.

A bootstrap capacitor provides the above-battery supply voltage required for N-channel MOSFETs. An internal charge pump for the high side allows for dc (100% duty cycle) operation of the half-bridge.

The A3946 is available in a choice of two power packages: a 16-lead SOIC with copper batwing power tab (part number suffix *LB*), and a 16-lead TSSOP with exposed thermal pad (suffix *LP*).

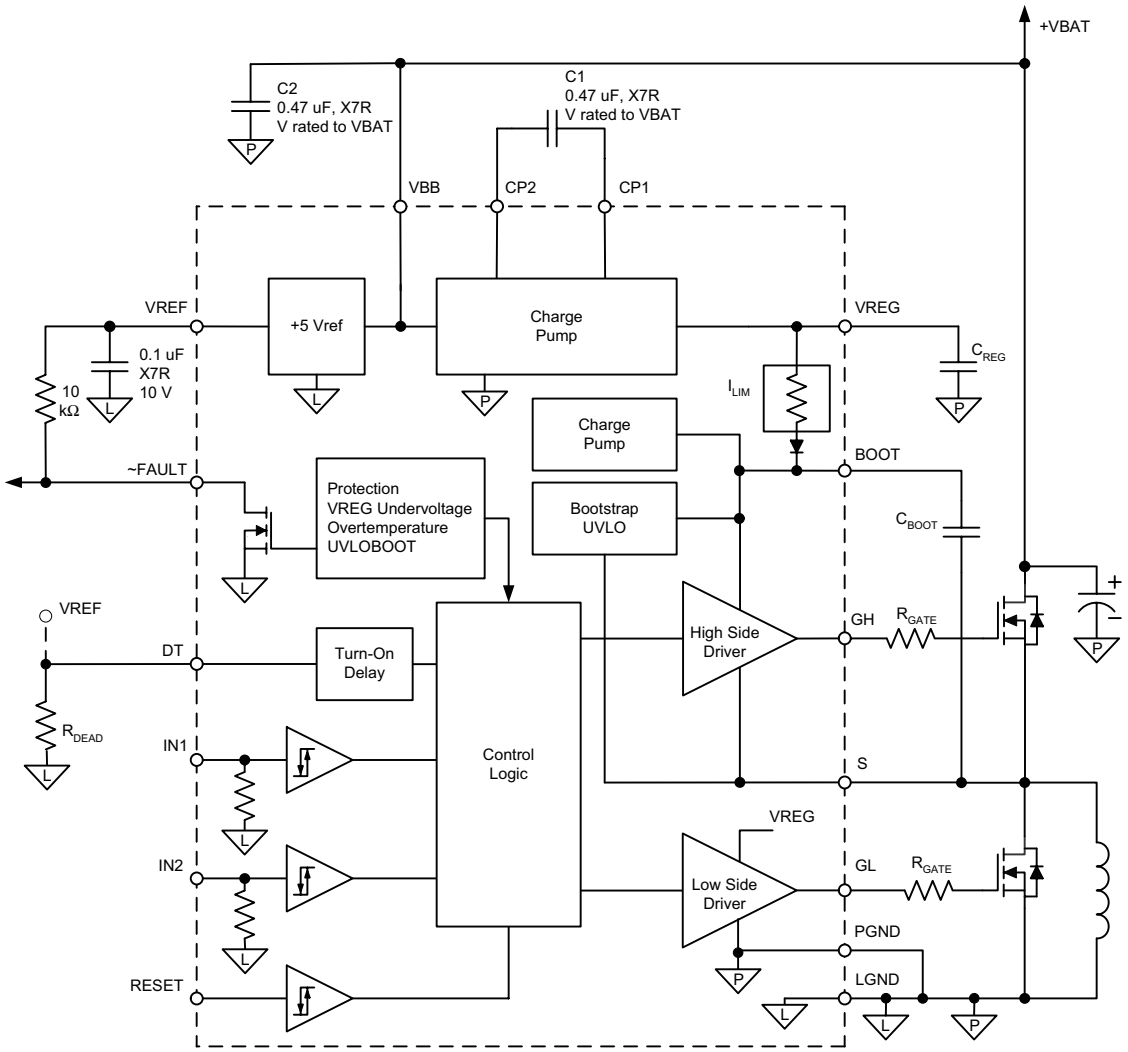
FEATURES

- On-chip charge pump for 7 V minimum input supply voltage
- High-current gate drive for driving a wide range of N-channel MOSFETs
- Bootstrapped gate drive with charge pump for 100% duty cycle
- Overtemperature protection
- Undervoltage protection
- –40ºC to 135ºC ambient operation

Always order by complete part number:

Part Number	Package
A3946KLB	16-Lead SOIC; Copper Batwing Power Tab
A3946KLP	16-Lead TSSOP; Exposed Thermal Pad

Functional Block Diagram



Control Logic Table

IN1	IN2	DT Pin	RESET	GH	GL	Function
X	X	X	0	Z	Z	Sleep mode
0	0	R_{DEAD} - LGND	1	L	H	Low-side FET ON following dead time
0	1	R_{DEAD} - LGND	1	L	L	All OFF
1	0	R_{DEAD} - LGND	1	L	L	All OFF
1	1	R_{DEAD} - LGND	1	H	L	High-side FET ON following dead time
0	0	VREF	1	L	L	All OFF
0	1	VREF	1	L	H	Low-side FET ON
1	0	VREF	1	H	L	High-side FET ON
1	1	VREF	1	H	H	CAUTION: High-side and low-side FETs ON

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ELECTRICAL CHARACTERISTICS at T_A = –40 to +135°C, V_{BB} = 7 to 60 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
V_{BB} Quiescent Current	I_{VBB}	RESET = High, Outputs Low	—	3	6	mA
		RESET = Low	—	—	10	µA
VREG Output Voltage	V_{REG}	V_{BB} > 7.75 V, I_{reg} = 0 mA to 15 mA	12.0	13	13.5	V
		V_{BB} = 7 V to 7.75 V, I_{reg} = 0 mA to 15 mA	11.0	—	13.5	V
Charge Pump Frequency	F_{CP}	CP1, CP2	—	62.5	—	kHz
VREF Output Voltage	V_{REF}	I_{REF} ≤ 4 mA, C_{REF} = 0.1 µF	4.5	—	5.5	V
Gate Output Drive						
Turn On Time	t_{rise}	C_{LOAD} = 3300 pF, 20% to 80%	—	60	100	ns
Turn Off Time	t_{fall}	C_{LOAD} = 3300 pF, 80% to 20%	—	40	80	ns
Pullup On Resistance	R_{DSUP}	T_j = 25°C	—	4	—	Ω
		T_j = 135°C	—	6	—	Ω
Pulldown On Resistance	R_{DSDOWN}	T_j = 25°C	—	2	—	Ω
		T_j = 135°C	—	3	—	Ω
Short Circuit Current – Source	—	t_{pw} < 10 µs	800	—	—	mA
Short Circuit Current – Sink	—	t_{pw} < 10 µs	1000	—	—	mA
GH Output Voltage	V_{GH}	t_{pw} < 10 µs, Bootstrap Capacitor fully charged	V_{REG} – 1.5	—	—	V
GL Output Voltage	V_{GL}	—	V_{REG} – 0.2	—	—	V
Timing						
Dead Time (Delay from Turn Off to Turn On)	t_{DEAD}	R_{dead} = 5 kΩ	200	350	500	ns
		R_{dead} = 100 kΩ	5	6	7	µs
Propagation Delay	t_{PD}	Logic input to unloaded GH, GL. DT = VREF	—	—	150	ns

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Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Protection						
VREG Undervoltage	V_{REGON}	V_{REG} increasing	8.6	9.1	9.6	V
VREG Undervoltage	V_{REGOFF}	V_{REG} decreasing	7.8	8.3	8.8	V
BOOT Undervoltage	V_{BSON}	V_{BOOT} increasing	8	8.75	9.5	V
BOOT Undervoltage	V_{BSOFF}	V_{BOOT} decreasing	7.25	8.0	8.75	V
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	—	170	—	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	—	15	—	°C
Logic						
Input Current	$I_{IN(1)}$	IN1 V_{IN} / IN2 V_{IN} = 2.0 V	—	40	100	µA
	$I_{IN(0)}$	IN1 V_{IN} / IN2 V_{IN} = 0.8 V	—	16	40	µA
		RESET pin only	—	—	1	µA
Logic Input Voltage	$V_{IN(1)}$	IN1 / IN2 logic high	2.0	—	—	V
		RESET logic high	2.2	—	—	V
	$V_{IN(0)}$	Logic low	—	—	0.8	V
Logic Input Hysteresis	—	All digital inputs	100	—	300	mV
Fault Output	V_{ol}	I = 1 mA, fault asserted	—	—	400	mV
	V_{oh}	V = 5 V	—	—	1	µA

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Functional Description

VREG. A 13 V output from the on-chip charge pump, used to power the low-side gate drive circuit directly, provides the current to charge the bootstrap capacitors for the high-side gate drive.

The VREG capacitor, C_{REG}, must supply the instantaneous current to the gate of the low-side MOSFET. A 10 µF, 25 V capacitor should be adequate. This capacitor can be either electrolytic or ceramic (X7R).

Diagnostics and Protection. The fault output pin, ~FAULT, goes low (i.e., FAULT = 1) when the RESET line is high and any of the following conditions are present:

- Undervoltage conditions on VREG (UVREG) or on the internal logic supply VREF (UVREF). These conditions set a latched fault.
- A junction temperature > 170°C (OVERTEMP). This condition sets a latched fault.
- An undervoltage on the stored charge of the BOOT capacitor (UVBOOT). This condition does NOT set a latched fault.

An overtemperature event signals a latched fault, but does not disable any output drivers, regulators, or logic inputs. The user must turn off the A3946 (e.g., force the RESET line low) to prevent damage.

The power FETs are protected from inadequate gate drive voltage by undervoltage detectors. Either of the regulator undervoltage faults (UVREG or UVREF) disable both output drivers until both voltages have been restored. The high-side driver is also disabled during a UVBOOT fault condition.

Under many operating conditions, both the high-side (GH) and low-side (GL) drivers may be off, allowing the BOOT capacitor to discharge (or never become charged) and create a UVBOOT fault condition, which in turn inhibits the high-side driver and creates a FAULT = 1. This fault is NOT latched. To remove this fault, momentarily turn on GL to charge the BOOT capacitor.

Latched faults may be cleared by a low pulse, 1 to 10 µs wide, on the RESET line. Throughout that pulse (despite a possible UVBOOT), FAULT = 0; also the fault latch is cleared immediately, and remains cleared. If the power is restored (no UVREG or UVREF), and if no OVERTEMP fault exists, then the latched fault remains cleared when the RESET line returns to high. However, FAULT = 1 may still occur because a UVBOOT fault condition may still exist.

Charge Pump. The A3946 is designed to accommodate a wide range of power supply voltages. The charge pump output, VREG, is regulated to 13 V nominal.

In all modes, this regulator is current-limited. When V_{BB} < 8 V, the charge pump operates as a voltage doubler. When 8 V < V_{BB}< 15 V, the charge pump operates as a voltage doubler/PWM, current-controlled, voltage regulator. When V_{BB}>15 V, the charge pump operates as a PWM, current-controlled, voltage regulator. Efficiency shifts, from 80% at V_{BB}= 7 V, to 20% at V_{BB} = 50 V.

CAUTION. Although simple paralleling of VREG supplies from several A3946s may appear to work correctly, such a configuration is NOT recommended. There is no assurance that one of the regulators will not dominate, taking on all of the load and back-biasing the other regulators. (For example, this could occur if a particular regulator has an internal reference voltage that is higher that those of the other regulators, which would force it to regulate at the highest voltage.)

Sleep Mode/Power Up. In Sleep Mode, all circuits are disabled in order to draw minimum current from VBB. When powering up and leaving Sleep Mode (the RESET line is high), the gate drive outputs stay disabled and a fault remains asserted until VREF and VREG pass their undervoltage thresholds. When powering up, before starting the first bootstrap charge cycle, wait until $t = C_{REG}/4$ (where C_{REG} is in µF, and t is in ns) to allow the charge pump to stabilize.

When powered-up (not in Sleep Mode), if the RESET line is low for > 10 µs, the A3946 may start to enter Sleep Mode (V_{REF} < 4 V). In that case, ~FAULT = 1 as long as the RESET line remains low.

If the RESET line is open, the A3946 should go into Sleep Mode. However, to ensure that this occurs, the RESET line must be grounded.

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Dead Time. The analog input pin DT sets the delay to turn on the high- or low-side gate outputs. When instructed to turn off, the gate outputs change after an short internal propagation delay (90 ns typical). The dead time controls the time between this turn-off and the turn-on of the appropriate gate. The duration, t_{DEAD}, can be adjusted within the range 350 ns to 6000 ns using the following formula:

$$t_{DEAD} = 50 + (R_{DEAD} / 16.7)$$

where t_{DEAD} is in ns, and R_{DEAD} is in Ω, and should be in the range 5 kΩ < R_{DEAD} < 100 kΩ.

Do not ground the DT pin. If the DT pin is left open, dead time defaults to 12 µs.

Control Logic. Two different methods of control are possible with the A3946. When a resistor is connected from DT to ground, a single-pin PWM scheme is utilized by shorting IN1 with IN2. If a very slow turn-on is required (greater than 6 µs), the two input pins can be hooked-up individually to allow the dead times to be as long as needed.

The dead time circuit can be disabled by tying the DT pin to VREF. This disables the turn-on delay and allows direct control of each MOSFET gate via two control lines. This is shown in the Control Logic table, on page 2.

Top-Off Charge Pump. An internal charge pump allows 100% duty cycle operation of the high-side MOSFET. This is a low-current trickle charge pump, and is only operated after a high-side has been signaled to turn on. A small amount of bias current (< 200 µA) is drawn from the BOOT pin to operate the floating high-side circuit. The charge pump simply provides enough drive to ensure that the gate voltage does not droop due to this bias supply current. The charge required for initial turn-on of the high-side gate must be supplied by bootstrap capacitor charge cycles. This is described in the section Application Information.

VREF. VREF is used for the internal logic circuitry and is not intended as an external power supply. However, the VREF pin can source up to 4 mA of current. A 0.1 µF capacitor is needed for decoupling.

Fault Response Table

Fault Mode	RESET	~FAULT	VREG	VREF	GH[1]	GL[1]
No Fault	1	1	ON	ON	(IL)	(IL)
BOOT Capacitor Undervoltage[2]	1	0	ON	ON	0	(IL)
VREG Undervoltage[3]	1	0	ON	ON	0	0
VREF Undervoltage[4]	1	0	OFF	ON	0	0
Thermal Shutdown[3]	1	0	ON	ON	(IL)	(IL)
Sleep[5]	0	1	OFF	OFF	High Z	High Z

[1](IL) indicates that the state is determined by the input logic.
[2]This fault occurs whenever there is an undervoltage on the BOOT capacitor. This fault is not latched.
[3]These faults are latched. Clear by pulsing RESET = 0.
[4]Unspecified VREF undervoltage threshold < 4 V.
[5]During power supply undervoltage conditions, GH and GL are instructed to be 0 (low). However, with VREG < 4 V, the outputs start to become high impedance (High Z). Refer to the section *Sleep Mode/Power Up*.

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Application Information

Bootstrap Capacitor Selection. C_{BOOT} must be correctly selected to ensure proper operation of the device. If too large, time is wasted charging the capacitor, with the result being a limit on the maximum duty cycle and PWM frequency. If the capacitor is too small, the voltage drop can be too large at the time the charge is transferred from the C_{BOOT} to the MOSFET gate.

To keep the voltage drop small:

$$Q_{BOOT} >> Q_{GATE}$$

where a factor in the range of 10 to 20 is reasonable. Using 20 as the factor:

$$Q_{BOOT} = C_{BOOT} \times V_{BOOT} = Q_{GATE} \times 20$$

and

$$C_{BOOT} = Q_{GATE} \times 20 / V_{BOOT}$$

The voltage drop on the BOOT pin, as the MOSFET is being turned on, can be approximated by:

$$Delta_v = Q_{GATE} / C_{BOOT}$$

For example, given a gate charge, Q_{GATE}, of 160 nC, and the typical BOOT pin voltage of 12 V, the value of the Boot capacitor, C_{BOOT}, can be determined by:

$$C_{BOOT} = (160\ nC \times 20) / 12\ V \approx 0.266\ \mu F$$

Therefore, a 0.22 µF ceramic (X7R) capacitor can be chosen for the Boot capacitor.

In that case, the voltage drop on the BOOT pin, when the high-side MOSFET is turned on, is:

$$Delta_v = 160\ nC / 0.22\ \mu F = 0.73\ V$$

Bootstrap Charging. It is good practice to ensure that the high-side bootstrap capacitor is completely charged before a high-side PWM cycle is requested.

The time required to charge the capacitor can be approximated by:

$$t_{CHARGE} = C_{BOOT} (Delta_v / 100\ mA)$$

At power-up and when the drivers have been disabled for a long time, the bootstrap capacitor can be completely discharged. In this case, Delta_v can be considered to be the full high-side drive voltage, 12 V. Otherwise, Delta_v is the amount of voltage dropped during the charge transfer, which should be 400 mV or less. The capacitor is charged whenever the S pin is pulled low, via a GL PWM cycle, and current flows from VREG through the internal bootstrap diode circuit to C_{BOOT}.

Power Dissipation. For high ambient temperature applications, there may be little margin for on-chip power consumption. Careful attention should be paid to ensure that the operating conditions allow the A3946 to remain in a safe range of junction temperature.

The power consumed by the A3946 can be estimated as:

$$P_total = Pd_bias + Pd_cpump + Pd_switching_loss$$

where:

$Pd_bias = V_{BB} \times I_{VBB}$, typically 3 mA,

and

$Pd_cpump = (2V_{BB} - V_{REG})\ I_{AVE}$, for $V_{BB} < 15$ V, or

$Pd_cpump = (V_{BB} - V_{REG})\ I_{AVE}$, for $V_{BB} > 15$ V,

in either case, where

$$I_{AVE} = Q_{GATE} \times 2 \times f_{PWM}$$

and

$Pd_switching_loss = Q_{GATE} \times V_{REG} \times 2 \times f_{PWM}$ Ratio,

where

$$Ratio = 10\ \Omega / (R_{GATE} + 10\ \Omega).$$

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Application Block Diagrams

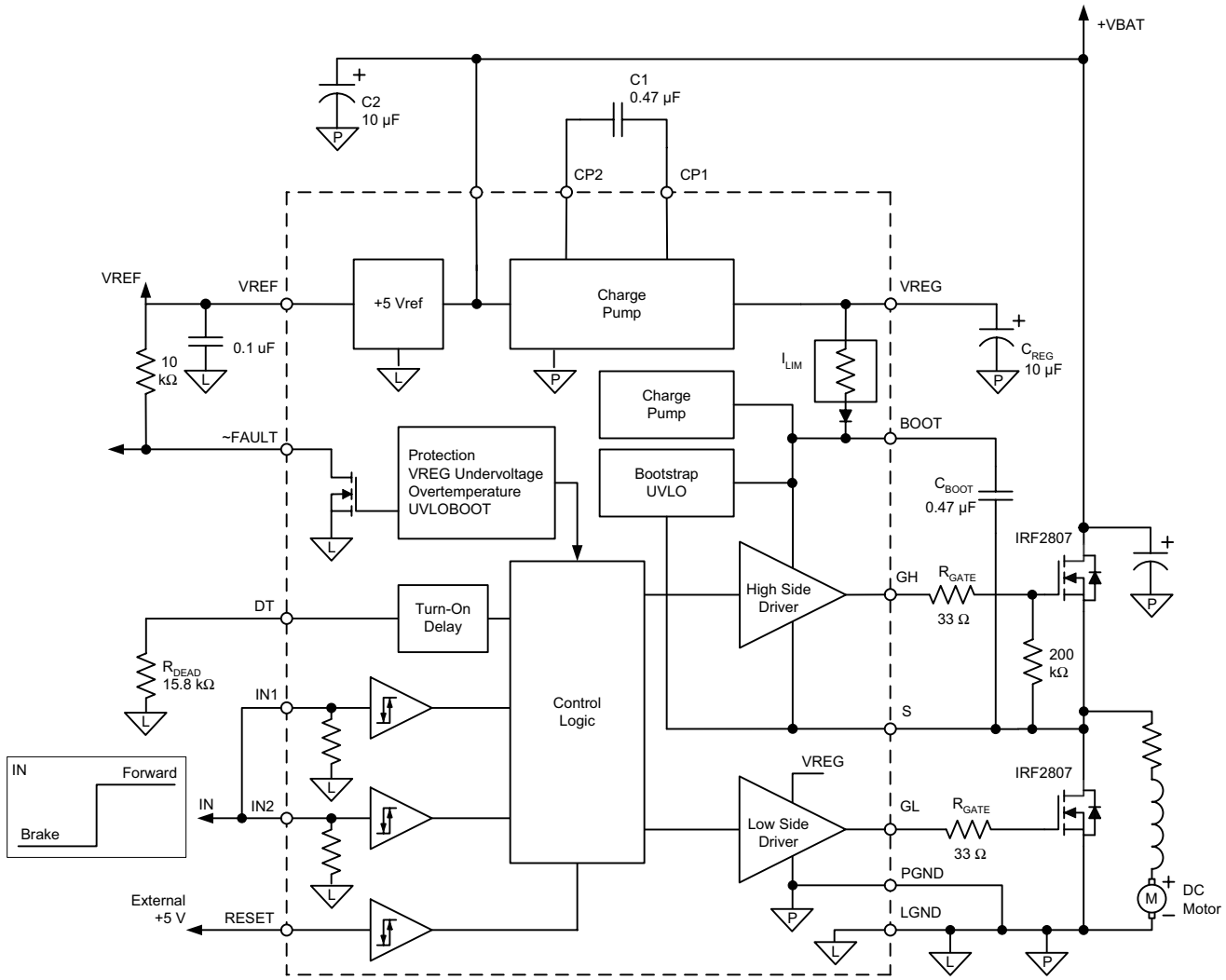

Diagram A. Dependent drivers. Unidirectional motor control with braking and dead time. T_{DEAD} = 1 µs; Q_{TOTAL} = 160 nC.

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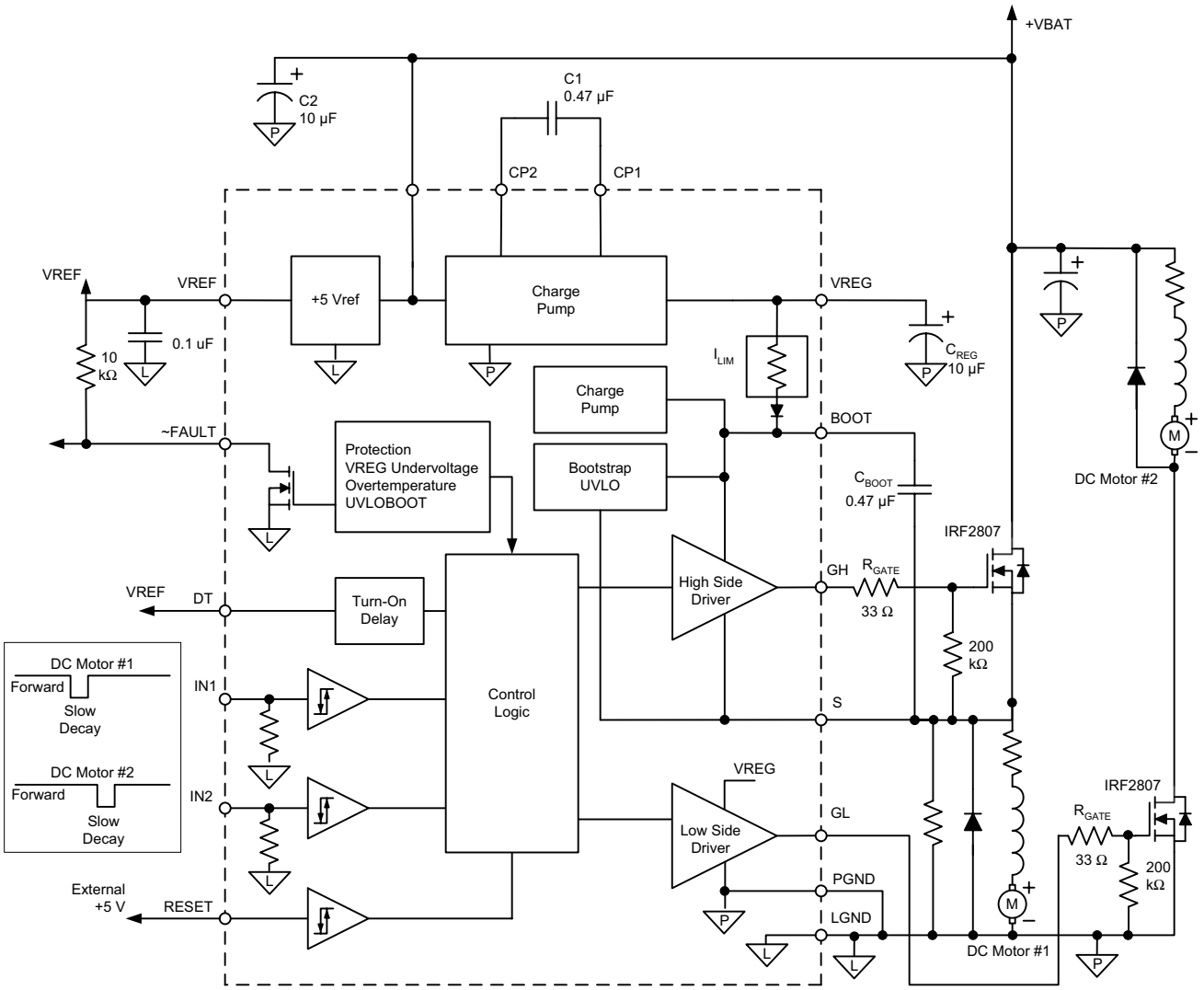

Diagram B. Independent drivers. One high-side drive and one low-side drive.

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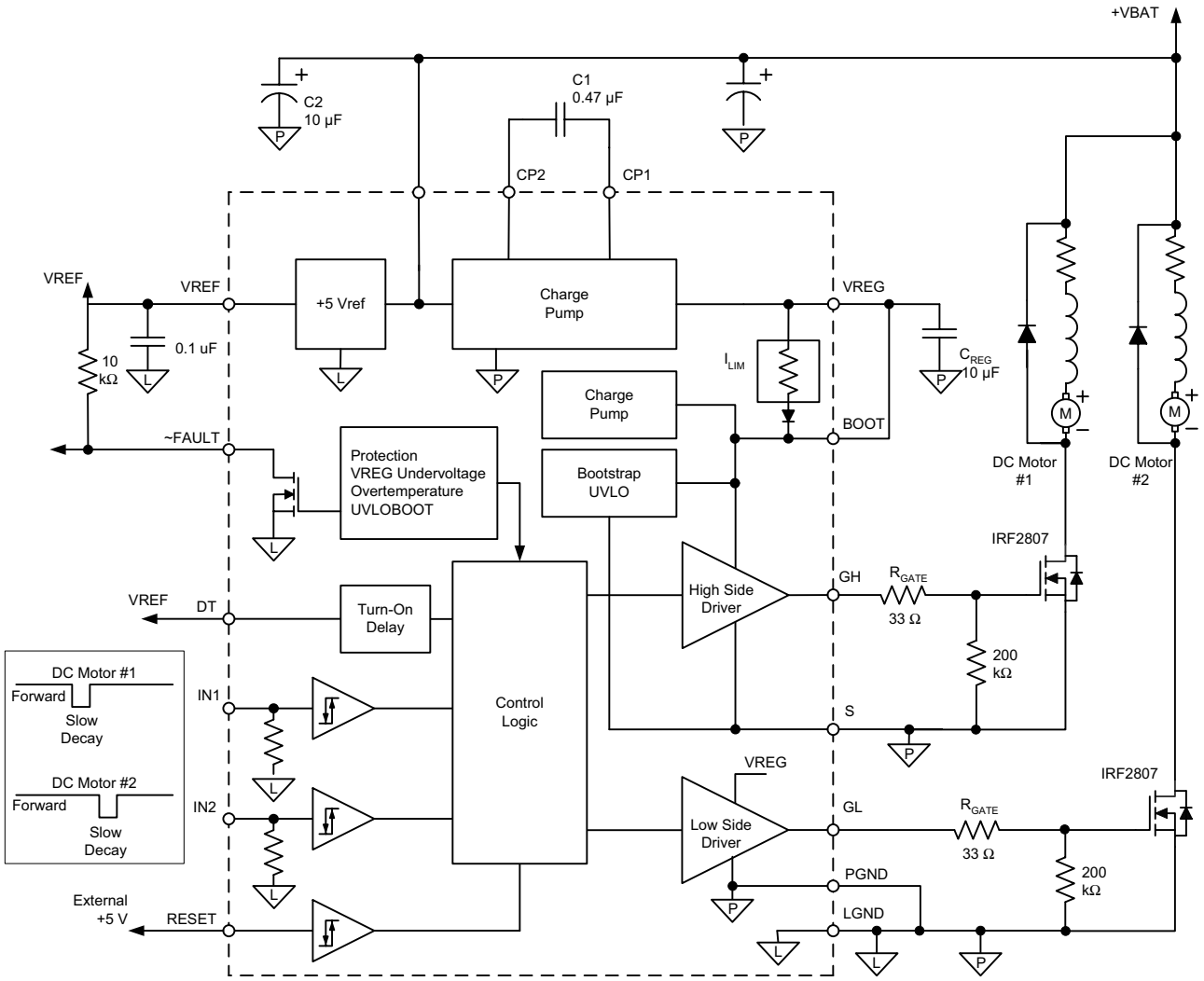

Diagram C. Independent drivers. Two low-side drives.

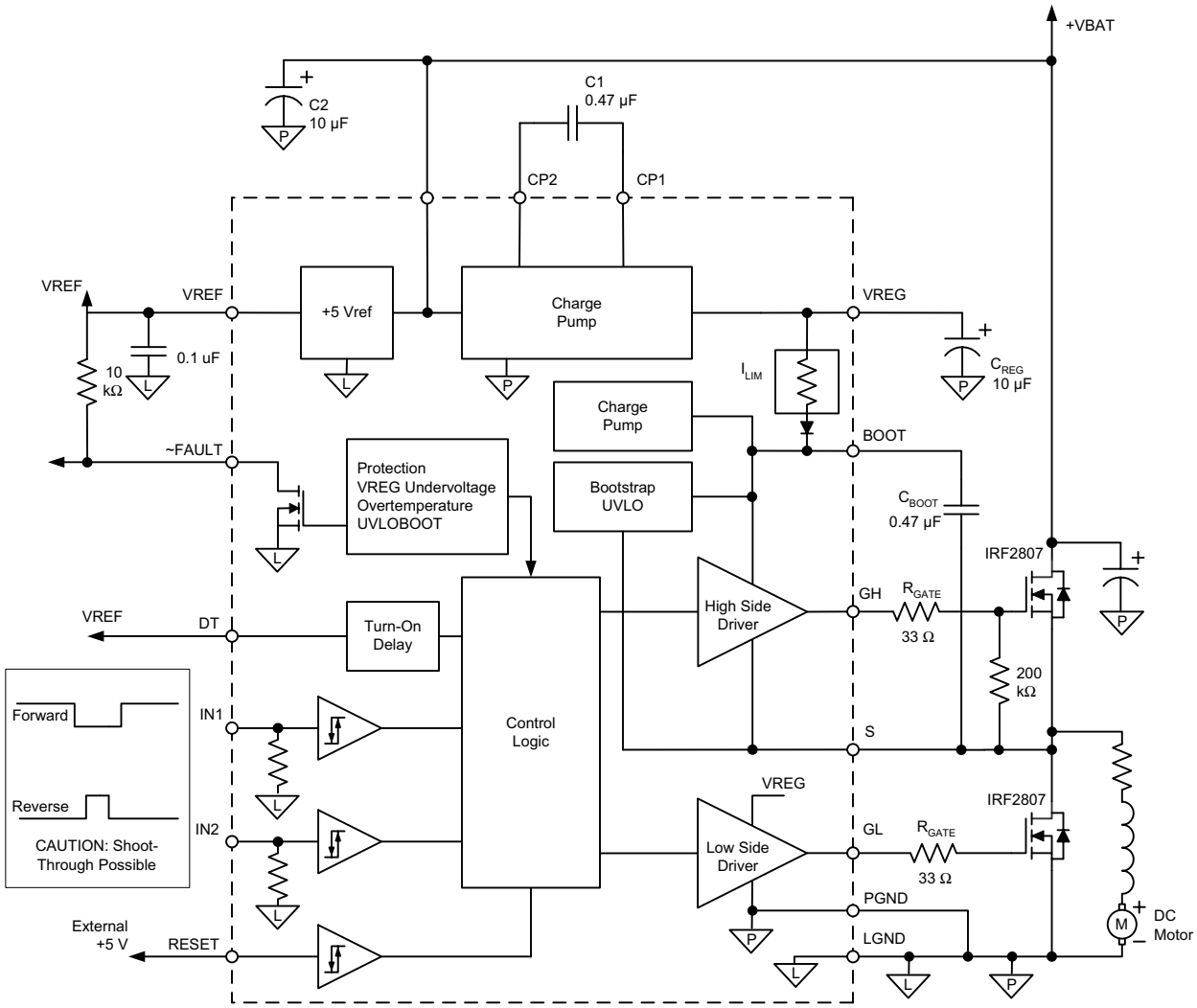

Diagram D. Dependent drivers with independent controls. Unidirectional, motor control with brake/coast, but without dead time control.

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Pin Name	Pin Description	SOIC-16 (A3946KLB)	TSSOP-16 (A3946KLP)
VREG	Gate drive supply.	1	1
CP2	Charge pump capacitor, positive side. When not using the charge pump, leave this pin open.	2	2
CP1	Charge pump capacitor, negative side. When not using the charge pump, leave this pin open.	3	3
PGND*	External ground. Internally connected to the power ground.	4	4
GL	Low-side gate drive output for external MOSFET driver. External series gate resistor can be used to control slew rate seen at the power driver gate, thereby controlling the di/dt and dv/dt of the S pin output.	5	5
S	Directly connected to the load terminal. The pin is also connected to the negative side of the bootstrap capacitor and negative supply connection for the floating high-side drive.	6	6
GH	High-side gate drive output for N-channel MOSFET driver. External series gate resistor can be used to control slew rate seen at the power driver gate, thereby controlling the di/dt and dv/dt of the S pin output.	7	7
BOOT	High-side connection for bootstrap capacitor, positive supply for the high-side gate drive.	8	8
~FAULT	Diagnostic output, open drain. Low during a fault condition.	9	9
IN1	Logic control.	10	10
IN2	Logic control.	11	11
RESET	Logic control input. When RESET = 0, the chip is in a very low power sleep mode.	12	12
LGND*	External ground. Internally connected to the logic ground.	13	13
DT	Dead Time. Connecting a resistor to GND sets the turn-on delay to prevent shoot-through. Forcing this input high disables the dead time circuit and changes the logic truth table.	14	14
VREF	5 V internal reference decoupling terminal.	15	15
VBB	Supply Input.	16	16

*In the LB package, the PGND pin (4) and LGND pin (13) grounds are internally connected by the leadframe. In the LP package, however, the PGND pin (4) and LGND pin (13) grounds are NOT internally connected, and both must be connected to ground externally.

In the LP package, the exposed thermal pad is not connected to any pin, but should be externally connected to ground, to reduce noise pickup by the pad.

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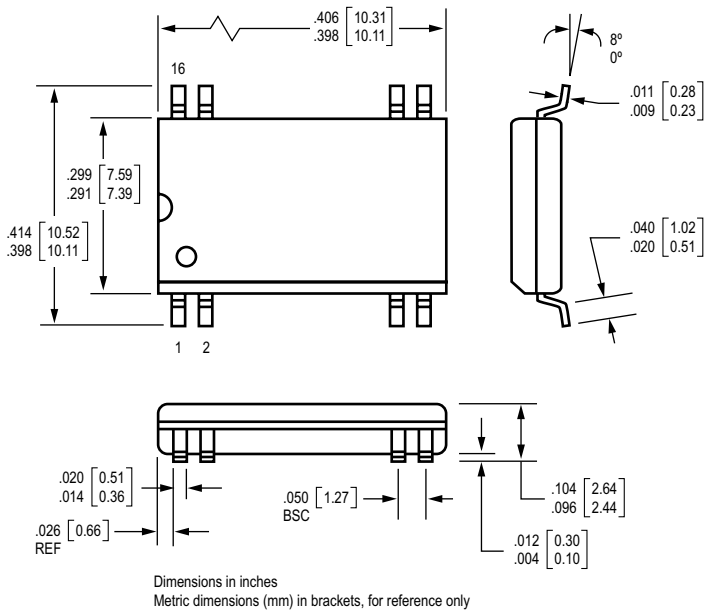
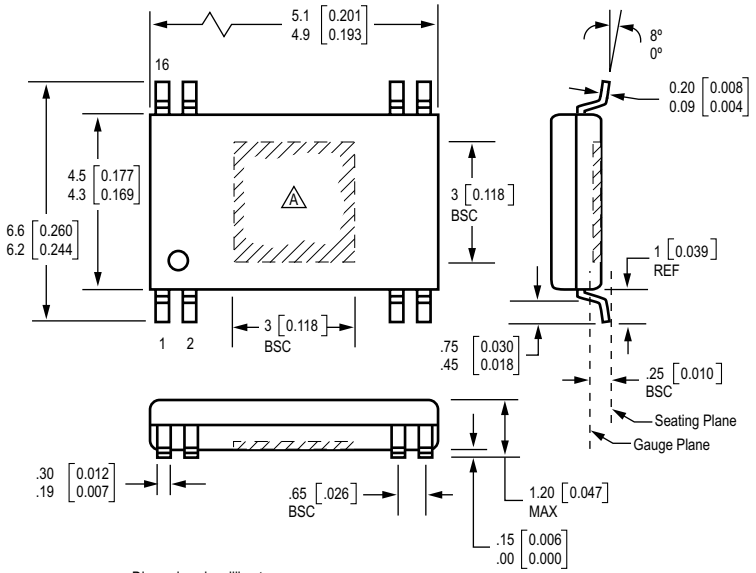


Dimensions in inches
Metric dimensions (mm) in brackets, for reference only

Webbed lead frame. Leads 4 and 13 are joined together within the device package.

A3946KLP TSSOP with Exposed Thermal Pad



Dimensions in millimeters
U.S. Customary dimensions (in.) in brackets, for reference only
A Exposed thermal pad (bottom surface)

NOTES:
1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Supplied in standard sticks/tubes of 49 devices or add "TR" to part number for tape and reel.

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Half-Bridge Power MOSFET Controller

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